MEWAR UNIVERSITY CHITTORGARH (RAJASTHAN)

Faculty of Engineering and Technology

Scheme and Syllabus of

Master of Technology (Part-time)
VLSI Design
MEWAR UNIVERSITY CHITTORGARH (RAJASTHAN)
Faculty of Engineering and Technology

Three-Year (Part-time) M Tech: VLSI Design

**Eligibility for Admission:** A candidate for being eligible for admission to the Master of Technology in *VLSI Design* in the faculty of engineering and technology should have passed B.Sc. (Engg.)/ B.Tech/ B.E. or any other equivalent degree in the relevant discipline / branch from any recognized Indian or foreign University.

A candidate should have at least 55% marks or equivalent CGPA in the qualifying examination (50% marks or equivalent CGPA for Scheduled Caste/Scheduled Tribes Candidates) on the basis of which the admission is being sought.

**Overview of the Programme:** The normal duration of programme shall be Six Semesters for part-time students. A part time candidate shall mean a person employed in any government/ semi-government/ private organisation. The duration of the programme is extendable upto five years. However, in exceptional circumstances one-year extension may be granted with approval of the Vice-Chancellor of the University.

The complete programme comprises of 13 theory courses (09 Core and 04 elective) and 02 Lab courses followed by the dissertation in two phases. Student has to obtain at least 40 % marks to pass the examination (both internal and external examination separately) for all the courses specified in the scheme of the programme. The degree will be awarded on the basis of cumulative marks obtained in all the six semesters and the division obtained will be as under:
<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Title</th>
<th>Contact Hours per week</th>
<th>Credit Hours</th>
<th>Internal Assessment/Examination</th>
<th>External Examination/Viva-voce</th>
<th>Total Marks</th>
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<tbody>
<tr>
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<td></td>
<td>L</td>
<td>P</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VD-611</td>
<td>Semiconductor Device Modelling</td>
<td>4</td>
<td>-</td>
<td>4</td>
<td>30</td>
<td>10</td>
</tr>
<tr>
<td>VD-613</td>
<td>Digital IC Design</td>
<td>4</td>
<td>-</td>
<td>4</td>
<td>30</td>
<td>10</td>
</tr>
<tr>
<td>VD-711/713/715</td>
<td>Elective-I</td>
<td>3</td>
<td>-</td>
<td>3</td>
<td>20</td>
<td>10</td>
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<tr>
<td>VD-617</td>
<td>Digital Design Lab</td>
<td>-</td>
<td>2</td>
<td>2</td>
<td>15</td>
<td>10</td>
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**Total Semester Credits = 13**

**Total Semester Marks = 325**

<table>
<thead>
<tr>
<th>Course Code</th>
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<td>L</td>
<td>P</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>VD-612</td>
<td>HDLs and FPGAs</td>
<td>4</td>
<td>-</td>
<td>4</td>
<td>30</td>
<td>10</td>
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<tr>
<td>VD-614</td>
<td>Analog IC Design</td>
<td>4</td>
<td>-</td>
<td>4</td>
<td>30</td>
<td>10</td>
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<tr>
<td>VD-712/714/716</td>
<td>Elective-II</td>
<td>3</td>
<td>-</td>
<td>3</td>
<td>20</td>
<td>10</td>
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<tr>
<td>VD-618</td>
<td>Analog Design Lab</td>
<td>-</td>
<td>2</td>
<td>2</td>
<td>15</td>
<td>10</td>
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**Total Semester Credits = 13**

**Total Semester Marks = 325**
### Third Semester

<table>
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<tr>
<th>Course Code</th>
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<th>Internal Assessment/Examination</th>
<th>External Examination/Viva-voce</th>
<th>Total Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>VD-615</td>
<td>Embedded Systems</td>
<td>4 L - 4 P</td>
<td>30</td>
<td>10</td>
<td>60</td>
<td>100</td>
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<tr>
<td>VD-621</td>
<td>Digital system Testing &amp; Testable Design</td>
<td>4 L - 4 P</td>
<td>30</td>
<td>10</td>
<td>60</td>
<td>100</td>
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<tr>
<td>VD-721/723/725</td>
<td>Elective-III</td>
<td>3 L - 3 P</td>
<td>20</td>
<td>10</td>
<td>45</td>
<td>75</td>
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**Total Semester Credits = 11**  
**Total Semester Marks = 275**

### Fourth Semester

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Title</th>
<th>Contact Hours per week</th>
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<th>External Examination/Viva-voce</th>
<th>Total Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>VD-616</td>
<td>Digital Signal Processing and DSP Architectures</td>
<td>4 L - 4 P</td>
<td>30</td>
<td>10</td>
<td>60</td>
<td>100</td>
</tr>
<tr>
<td>VD-624</td>
<td>Optimization Techniques</td>
<td>4 L - 4 P</td>
<td>30</td>
<td>10</td>
<td>60</td>
<td>100</td>
</tr>
<tr>
<td>VD-722/724/726</td>
<td>Elective-IV</td>
<td>3 L - 3 P</td>
<td>20</td>
<td>10</td>
<td>45</td>
<td>75</td>
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</tbody>
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**Total Semester Credits = 11**  
**Total Semester Marks = 275**
### Fifth Semester

<table>
<thead>
<tr>
<th>Course Code</th>
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<th>Contact Hours per week</th>
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<th>Internal Assessment/Examination</th>
<th>External Examination/Viva-voce</th>
<th>Total Marks</th>
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<tbody>
<tr>
<td>VD – 627</td>
<td>Research Methodology</td>
<td>2</td>
<td>2</td>
<td>15</td>
<td>05</td>
<td>30</td>
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<tr>
<td>VD – 629</td>
<td>Dissertation (Phase-I)</td>
<td>-</td>
<td>6</td>
<td>75</td>
<td>75</td>
<td>150</td>
</tr>
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**Total Semester Credits = 08**  **Total Semester Marks = 200**

### Sixth Semester

<table>
<thead>
<tr>
<th>Course Code</th>
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<th>Contact Hours per week</th>
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<th>External Examination/Viva-voce</th>
<th>Total Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>VD – 630</td>
<td>Dissertation (Phase-II)</td>
<td>-</td>
<td>10</td>
<td>50</td>
<td>-</td>
<td>200</td>
</tr>
</tbody>
</table>

**Total Semester Credits = 10**  **Total Semester Marks = 250**
# LIST OF ELECTIVES

## ELECTIVE – I

<table>
<thead>
<tr>
<th></th>
<th>Course Code</th>
<th>Course Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>VD-711</td>
<td>Asynchronous System Design</td>
</tr>
<tr>
<td>2.</td>
<td>VD-713</td>
<td>Low-Power VLSI Design</td>
</tr>
<tr>
<td>3.</td>
<td>VD-715</td>
<td>Memory Design and Testing</td>
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</table>

## ELECTIVE – II

<table>
<thead>
<tr>
<th></th>
<th>Course Code</th>
<th>Course Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>VD-712</td>
<td>RF Integrated Circuits</td>
</tr>
<tr>
<td>2.</td>
<td>VD-714</td>
<td>Advanced Computational Methods</td>
</tr>
<tr>
<td>3.</td>
<td>VD-716</td>
<td>FPGA Based System Design</td>
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## ELECTIVE – III

<table>
<thead>
<tr>
<th></th>
<th>Course Code</th>
<th>Course Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>VD-721</td>
<td>Mixed Signal IC Design</td>
</tr>
<tr>
<td>2.</td>
<td>VD-723</td>
<td>Advanced Computer Architecture</td>
</tr>
<tr>
<td>3.</td>
<td>VD-725</td>
<td>Neural Networks</td>
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</table>

## ELECTIVE – IV

<table>
<thead>
<tr>
<th></th>
<th>Course Code</th>
<th>Course Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>VD-722</td>
<td>Micro Electro Mechanical Systems</td>
</tr>
<tr>
<td>2.</td>
<td>VD-724</td>
<td>VLSI For Wireless Communication</td>
</tr>
<tr>
<td>3.</td>
<td>VD-726</td>
<td>Cryptography &amp; Network Security</td>
</tr>
</tbody>
</table>
**Internal Assessment/Examination:** The internal evaluation for all theory courses (40% of the total marks) will be based on the evaluation of three assignments provided during the semester and assessment of the teacher concerned. Similarly, the internal evaluation for all Lab courses (50% of the total marks) will be based on the evaluation of lab record and assessment of the teacher concerned.

**External Examination/Viva-voce:** For all the theory courses, there will be 08 (Eight) questions to be set by the external paper setter (nominated/approved by the competent authority) out of which the candidate will have to attempt 05 (Five) questions all carrying equal marks. Duration of each external examination will be three hours. Similarly, the external evaluation for all Lab courses (50% of the total marks) will be based on the evaluation/viva-voce conducted by an external examiner (from the relevant field) nominated/approved by the competent authority.

**Submission and Evaluation of Dissertation:**

a) A dissertation supervisor (s) having at least post-graduate qualification, from industry/research organization shall be assigned to the student approved by the competent authority. *In no case, the candidate can have more than two dissertation supervisors.*

b) Dissertation work (Phase-I) in 5th semester shall comprise of literature survey, problem formulation, finalization of goals to be achieved, outlines of the methodology to be used for achieving the targeted goals and final decision about S/W, H/W tools to be used for dissertation work in 6th semester. The entire work will be documented in the form of report.

c) Internal assessment of dissertation (Phase-I) in 5th semester will be made by the committee evaluating the report (50% weightage), oral presentation and response of the student in the discussion/presentation (50% weightage). The dissertation supervisor (s) shall be the member (s) of the committee.

d) The submission of dissertation (Phase-II) in 6th semester shall be allowed only after ensuring that the research work carried out by the candidate has attained the level of satisfaction of the ‘Dissertation Supervisor (s)’ and proof of communication/acceptance of the research paper (if any, and certified in the report) in the relevant refereed journal/conference.

e) The final dissertation external examination in 6th semester shall be taken by a panel of examiners comprising of concerned Supervisor (s), one external examiner (from the relevant field) nominated/approved by the competent authority. Hard copies of dissertation, one for each supervisor (s), examiner and the university/department, are required to be submitted by the student before the final dissertation external examination. The candidate shall appear before the examining committee for oral examination and presentation on the scheduled date.
Brief review of silicon devices & fabrication processes, Recent developments in microelectronic devices.

p-n junction- current flow mechanisms , DC , small signal, transient model under forward and reverse bias conditions, circuit models for different types of p-n junction diodes.

Bipolar junction transistor-current flow in BJT's, charge control models for BJT's, DC and small signal equivalent circuits, Gummel Poon mode, MEXTRAM model, HICUM model, second order effects- effects of non-uniform doping in the base, high injection, heavy doping effects in emitter, emitter crowding , non conventional BJT's- poly silicon emitter transistor, HBT.

MOSFETs: modeling of weak and strong inversion in three terminal and four terminal MOS transistors, effect of small dimensions- DIBL, charge sharing, channel length modulation, hot carrier effects. Small signal models of MOSFETs for low and medium frequencies, large signal modeling of MOS transistor in dynamic operation. Level 1, 2, 3, 4(BSIM) models, HSPICE Level 50 model.

Modeling for circuit simulation: types of models combining several effects into one physical model, parameter extraction, properties of good models

**Note:** The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

**Recommended Books:**

M TECH: VLSI DESIGN
VD-613 DIGITAL IC DESIGN

Internal Assessment/Evaluation: 40 Marks
External Examination: 60 Marks
Duration of Examination: 03 Hours


Design of CMOS Combinational Logic Gates: Static and dynamic CMOS Design, Speed and power dissipation in dynamic circuits, cascading of gates, designing logic for reduced supply voltages, simulation of logic circuits.

Design of CMOS Sequential Logic Circuits: Static and dynamic latches and registers, alternative register styles, pipelined sequential circuits, non-bistable sequential circuits.

Custom, Semi-custom, and Structured array design approaches: Cell Based Design – standard, compiled, macro cells, mega cells, ArrayBased Design – mask programmable and rewired arrays.

Coupling with Interconnects: Effects of Interconnect Parasitics, Advanced Interconnect techniques.

Timing issues in Digital Circuits: Timing classification, synchronous timing basics, sources of skew and jitter, clock distribution techniques, latch-based clocking, Self-timed circuit design, synchronizers and arbiters, clock synchronization using PLL.

Design of ALU- a case study: data paths, adder, multiplier, shifter, power and speed trade-off in data path structures, power management.

Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:

Verilog: basic concepts- Lexical conventions, data types, system tasks and compiler directives. Modules and ports. Gate level modeling- gate types, various types of gate delay specifications. Data flow modeling- assignments, delays, expressions, operators. Behavioral modeling- structured procedures, procedural assignments, timing controls, conditional statements, loops, sequential and parallel blocks, generate blocks. Tasks and functions

FPGA Architectures and Technology. Historical background, channel type FPGA- Xilinx 3000 and Actel ACT2 family, structured programmable array logic, programming FPGAs, benchmarking of FPGAs. Recent developments- new architectures such as Altera FLEX, Pilkington (Motorola/Toshiba), Xilinx XC4000, field programmable interconnect.


Verilog Synthesis for FPGA Implementation: Verilog constructs and operators, interpretation of Verilog constructs, synthesis design flow- RTL to gates, translation, un-optimized intermediate representations, logic optimization, technology mapping and optimization, technology library, design constraints, optimized gate level description.

Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:

- K. Coffman, Real World FPGA Design with Verilog, PH, 2000
Integrated CMOS Amplifiers: Why integrated CMOS, single stage amplifiers-common source amplifiers with different types of loads, source follower, common gate amplifiers, cascade stage, choice of device models, Differential amplifiers-analysis of single ended and differential output amplifiers, common mode response, differential pair with MOS load, gilbert cells.

Current Mirrors: Basic current mirrors, cascade current mirrors, analysis of current mirrors, Frequency response of amplifiers: general considerations, frequency response of different types of amplifiers, Sources of Noise in CMOS Amplifiers: types of noise, representation of noise, noise in amplifiers.

CMOS Band gap References: supply independent biasing, temperature independent references, PTAT current generation, constant $G_m$ biasing, speed and noise issues, Comparators.

Feedback in Amplifiers: feedback topologies, effect of loading, effect of feedback on noise, CMOS Operational Amplifiers-performance parameters, one-stage and two-stage Op Amps, gain boosting, input range limitations, slew rate.

Switched Capacitor Circuits: sampling switches, speed and precision considerations, switched capacitor amplifier –unity gain buffer, switched capacitor common mode feedback, switched capacitor filters.

CMOS Phase Lacked Loops: simple PLLs, charge pump PLLs, non ideal effects in PLLs, applications in frequency multiplication, skew and jitter reduction.

**Note:** The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

**Recommended Books:**

Laboratory Experiments:

1. Design and simulation of 8-bit SISO and SIPO type registers modeled in VHDL and VERILOG, and synthesis on FPGA.
2. Circuit simulation of CMOS Inverter - study of static and dynamic behavior.
3. Design and simulation of 8-bit PISO and PIPO type registers modeled in VHDL and VERILOG, and synthesis on FPGA.
4. Study of the effect of variation in $V_{DD}$ and Temperature on static and dynamic behavior of CMOS Inverter.
5. Design and simulation of 8:1 MUX modeled in VHDL and VERILOG, and synthesis on FPGA.
7. Design and simulation of 8-bit synchronous counter with LOAD, RESET, and up/down controls, modeled in VHDL and VERILOG, and synthesis on FPGA.
8. Layout design and characterization of master-slave DFF.
9. Design and simulation of 8-bit parity checker/generator modeled in VHDL and VERILOG, and synthesis on FPGA.
10. Layout design and characterization of NAND2 and NAND4 gates.
11. Design and simulation of 8:3 priority encoder, modeled in VHDL and VERILOG, and synthesis on FPGA.
12. Layout design and characterization of Transmission gate.
13. Design and simulation of 4-digit decade counter, modeled in VHDL and VERILOG, and synthesis on FPGA.
14. Design and simulation of 4-bit combinational multiplier, modeled in VHDL and VERILOG, and synthesis on FPGA.
15. Design and simulation of 4-bit sequential multiplier, modeled in VHDL and VERILOG, and synthesis on FPGA.
Laboratory Experiments:

1. Design and simulation of CS, CG and CD amplifier.
2. Design of a p-n junction, BJT and MOSFET using different process parameters.
3. Design and simulation of MOSFET based basic and cascade current mirrors.
4. Study of dependence of SPICE parameters on process parameters for BJT.
6. Study of dependence of SPICE parameters on process parameters for a MOSFET.
7. Design and simulation of a single stage CMOS operational amplifier.
8. Layout design and simulation of a differential amplifier.
10. Layout design and simulation of positive TC band gap reference.
11. Design and simulation of a second order switched capacitor filter.
12. Study of effect of short channel on SPICE parameters of a MOSFET.
15. Comparison of different device models using SPICE
M TECH: VLSI DESIGN

VD-615 EMBEDDED SYSTEM DESIGN

Internal Assessment/Evaluation: 40 Marks
External Examination: 60 Marks
Duration of Examination: 03 Hours


Processors: ARM and SHARC processors- processor and memory organization, data operations, flow of control, input and output devices and primitives, busy-wait I/O, interrupts, supervisor mode, exceptions, traps. Memories: Caches, MMUs and address translation; CPU Performance: pipelining, super scaling execution, caching, CPU power consumption.

Interfaces and Communication Mediums: Bus protocols, DMA, system bus configurations, ARM Bus, SHARC Bus, Memory Devices- organization and types, I/O Devices-timers and counters, ADC and DACs, keyboards, LEDs, Displays and touch screens, Interfacings-memory and device interfacing. Designing with microprocessors.


Examples and Case Studies.

Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:

- J. Catsoulis, Designing Embedded Hardware, ORA, 2002.
VD-621 DIGITAL SYSTEM TESTING & TESTABLE DESIGN

Internal Assessment/Evaluation: 40 Marks
External Examination: 60 Marks
Duration of Examination: 03 Hours

Combinational ATPG. Current sensing based testing. Classification of sequential ATPG methods. Fault collapsing and simulation

Universal test sets. Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.


Design for testability: Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives.

Built-in self-test: Estimation of test length, Test points to improve testability, Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing.

Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:

M TECH: VLSI DESIGN

VD-616 DIGITAL SIGNAL PROCESSING AND DSP ARCHITECTURES

Implementations of Basic DSP Operations - Adders, Multipliers, Dividers; Discrete Fourier Transform Implementation-characteristics of DFT- direct implementation of DFT, fast fourier transforms; Fixed-Point versus Floating-Point Operations; Pipelining and Parallelism; Re-timing, Unfolding- algorithm, properties and applications of unfolding, Folding- folding transformation, register minimization in folded architectures, folding of multirate systems.

Systolic/Array Architectures-implementation of array processors, algorithmic representations, Mapping methods-mapping without changing the number of nodes and with reduced number of nodes, projection method, multiprojection, partitioning, projection of nodes with different operations; Programmable DSP Architectures-the architecture of standard computer, architectural approaches for DSP processors, characteristics of available DSPs, FIR filter program, DFT program, instruction pipelining, special arithmetic modules, on-chip memory; Memory Structures and Addressing.

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P-DSP’s – Multiple access memory – Multi-port memory – VLIW architecture – pipelining – Special Addressing modes in P-DSP’s – On Chip Peripherals.

TMS320C3X PROCESSOR :Architecture –Data formats – Addressing modes – Groups of addressing modes – Instruction sets – Operation – Block diagram of DSP starter kit – Application, Programs for processing real time systems – Generating and finding the sum of series, Convolution of two sequences , Filter design.

ADSP PROCESSORS :Architecture of ADSP-21XX and ADSP – 210XX series of DSP processors – Addressing modes and Assembly language instructions – Applications programs – Filter design, FFT calculation- Blackfin DSP Processor

Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:

• User guides Texas Instrumentation, Analog Devices, Motorola.
M TECH: VLSI DESIGN

VD-624 Optimization Techniques

Internal Assessment/Evaluation: 40 Marks
External Examination: 60 Marks
Duration of Examination: 03 Hours

Artificial Neural Networks (ANN): Objectives—History—Biological inspiration, Neuron model, Single input neuron, Multi-input neuron, Network architecture, Single layer of neurons, Multi-layers of Neurons.

Perceptron: Perceptron architecture, Single-neuron perceptron, Multi-neuron perceptron—Perceptron Learning Rule, Constructing learning rules, Training multiple neuron perceptrons

Associative Learning: Simple associative network, Unsupervised Hebb-rule—Hebb rule with decay, Instar rule, Kohonen rule.


Applications for VLSI Design
Applications of Artificial Neural Networks to Function Approximation, Regression, Time Series and Forecasting.

Genetic Algorithms (GA): Introduction, robustness of traditional optimization and search methods, goals of optimization, difference between genetic algorithms and traditional methods, a simple genetic algorithm, hand simulation, Grist for the search mill, similarity templates, learning the lingo.

GA Mathematical Foundations: Foundation theorem, schema processing, the two armed and k-armed bandit problem, schemata processing, building block hypothesis, minimal deceptive problem (MDP), extended schema analysis, MDP results, similarity templates as hyper planes.

GA Computer Implementation: Introduction, data structures, reproduction, crossover and mutation, a time to reproduce and a time to cross, main program and results, mapping objective functions to fitness form, fitness scaling, codings, a multiparameter mapped fixed point coding, discretization, constraints.

Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:

M TECH: VLSI DESIGN

VD-627 Research Methodology

Internal Assessment/Evaluation: 20 Marks
External Examination: 30 Marks
Duration of Examination: 03 Hours

Introduction to Educational Research: Concept, types – basic, applied and action, Need for educational research;
Reviewing Literature: Need, Sources – Primary and Secondary, Purposes of Review, Scope of Review, steps in conducting review.
Identifying and defining research problem: Locating, analysing stating and evaluating problem. Generating different types of hypotheses and evaluating them.
Methods of Research: Descriptive research design - survey, case study, content analysis, Ex-post Facto Research, Correlational and Experimental Research
Sampling Techniques: Concept of population and sample’ sampling techniques - simple random sampling, stratified random sampling, systematic sampling and cluster sampling, snow ball sampling, purposive sampling, quota sampling techniques. determining size of sample.
Design and development of measuring instruments, Tests, questionnaires, checklists, observation schedules, evaluating research instruments, selecting a standardized test Procedure of data collection: Aspects of data collection, coding data for analysis.
Statistical Methods of Analysis: Descriptive statistics: Meaning, graphical representations, mean, range and standard deviation, characteristics and uses of normal curve. Inferential statistics: t-test, Chi-square tests, correlation (rank difference and product moment), ANOVA (one way), Selecting appropriate methods.
Procedure for writing a research proposal: Purpose, types and components of research proposal.
Procedure for writing a research report: Audiences and types of research reports, Format of research report and journal articles.
Strategies for evaluating, Research disseminating and utilising research – An Overview.

Practice Tasks
• Define a research problem in engineering education/industry after studying problem situation and literature
• Given the purpose, objectives of research, write hypotheses
• Select research designs for the given research objectives
• Identify the measuring instruments for the given research objectives/hypotheses
• Identify the appropriate statistical methods of analysis for the given research proposal.
• Critically analyse the given research reports on various aspects such as hypothesis, design, measuring tools, statistical analysis, interpretation etc. to identify the gaps or weaknesses in the study.
Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:
- CPSC: Developing Skills in Technician Education Research Modules 1 to 11 Singapore, Colombo Plan Staff College for Technician Education
The primary objective of this course is to enhance the student ability to analyze and carry out independent investigations etc. Each student will carry out independent work which should involve creativity; innovation and ingenuity. A dissertation supervisor (s) having at least post-graduate qualification; from industry/research organization shall be assigned to the student approved by the competent authority. *In no case; the candidate can have more than two dissertation supervisors.* Industry oriented projects may be encouraged for the purpose.

The whole Dissertation work will be carried out and reported in two phases in 5th semester and 6th semester. Dissertation work (Phase-I) in 5th semester shall comprise of literature survey; problem formulation; finalization of goals to be achieved; outlines of the methodology to be used for achieving the targeted goals and final decision about S/W; H/W tools to be used for dissertation work in 6th semester. The entire work will be documented in the form of report.

Internal assessment of dissertation (Phase-I) in 5th semester will be made by the committee evaluating the report (50% weightage); oral presentation and response of the student in the discussion / presentation (50% weightage). The dissertation supervisor (s) shall be the member (s) of the committee.
The complete dissertation work shall comprise of literature survey; problem formulation; methodology used; S/W; H/W tools used; Results and discussion followed by the conclusions & further scope of work in that area. The submission of dissertation in 6th semester shall be allowed only after ensuring that the research work carried out by the candidate has attained the level of satisfaction of the ‘Dissertation Supervisor(s)’ and proof of communication/acceptance of the research paper (if any; and certified in the report) in the relevant refereed journal/ conference.

The final dissertation external examination in 6th semester shall be taken by a panel of examiners comprising of concerned Supervisor(s); one external examiner (from the relevant field) nominated/approved by the competent authority. Hard copies of dissertation; one for each supervisor(s); examiner and the university/ department; are required to be submitted by the student before the final dissertation external examination. The candidate shall appear before the examining committee for oral examination and presentation on the scheduled date.
M TECH: VLSI DESIGN

VD-711 (ELECTIVE-I) ASYNCHRONOUS SYSTEM DESIGN

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Fundamentals: Handshake protocols, Muller C-element, Muller pipeline, Circuit implementation styles, theory. Static data-flow structures: Pipelines and rings, Building blocks, examples


High-level languages and tools: Concurrency and message passing in CSP, Tangram program examples, Tangram syntax-directed compilation, Martin’s translation process, Using VHDL for Asynchronous Design. An Introduction to Balsa: Basic concepts, Tool set and design flow, Ancillary Balsa Tools


Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:

M TECH: VLSI DESIGN
VD-713 (Elective-I)  Low-Power VLSI Design

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Introduction: Sources of power dissipation, important parameters for low power design, Low power design approaches.

Transistor sizing vs. dissipation and speed, effect of scaling, Process Technology and Integration-Low power CMOS/BiCMOS Process, Low power SOI CMOS, Low Power Lateral BJT on SOI, LVLP CMOS Transistor structure via Poly profile Engineering.


Low power clock distribution: Power Distribution in Clock Distribution, Single driver vs. Distributed buffers, Buffer and device sizing, Zero skew vs. tolerant Skew, Chip and package Co-design of Clock Network.


Design of low power arithmetic and memory elements: Circuit Design Style, Design of circuits for addition, Multiplication, Division.

Low power microprocessor Design – system power management, architectural trade-offs, choosing supply voltage, low power clocking, implementation options for low power.

Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:

M TECH: VLSI DESIGN

VD-715 (ELECTIVE-I)  MEMORY DESIGN AND TESTING

Internal Assessment/Evaluation:  30 Marks
External Examination:  45 Marks
Duration of Examination:  03 Hours

Introduction to Semiconductor Memories and Technologies: Internal organization of memory chips, basic memory elements, memory types, trends in SRAM and DRAM design, Non-volatile memory technologies.

SRAM and DRAM Cell Design; basic structures-NMOS static/dynamic circuits, CMOS circuits, cell design.

Sense Amplifiers: Voltage and Current Sense Amplifiers; Reference Voltage Generation; Voltage Converters.

Cache Memory Design.: concept of locality in space and time, interfacing cache memory with CPU, associated problems-parasitic capacitances, critical timing paths, bus turnaround.

Memory Testing: Reliability-failure mechanisms for memories, reliability modeling and fault detection, Yield, Radiation Effects-radiation types effecting the memory, radiation hardening techniques.

Memory chip design: a case study

Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:

M TECH: VLSI DESIGN

VD-712 (ELECTIVE-II) RF INTEGRATED CIRCUITS

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Active RF Components and their characteristic parameters: RF diodes, BJT, FET, HEMT.

RF Filter Design: Filter configurations, resonators, filter realizations – Butterworth, Chebychev.

High-Frequency Amplifier Design: Zeros as bandwidth enhancer, shunt series amplifier, bandwidth enhancement with \( f_T \) doublers, voltage references and biasing, tuned and cascaded amplifiers, RF Power Amplifier Design.

Noise in RF Circuits: types of noise, two port noise theory, Low-Noise Amplifier (LNA) – intrinsic MOSFET two port noise parameters, LNA topologies, design example, LNA Design example.

Phase-Locked Loops: PLL models, noise properties, sequential phase detectors, loop filters and charge pumps. RF Oscillators: tuned and negative resistance oscillators. Mixers: non-linear systems as mixers, multiplier based mixers.

RF amplifier design – a case study

Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:

Solution of two or more nonlinear equations by iterative methods (Picard and Newton’s methods) Spline interpolation, cubic splines, Chebyshev polynomials, Minimax approximation.


Numerical Solution of elliptic problems. Dirichlet and Neumann problems (Cartesian and Polar coordinates)


**Note:** The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

**Recommended Books:**

Multirate signal processing- Decimation and Interpolation. Spectrum of decimated and interpolated signals, Polyphase decomposition of FIR filters and its applications to multirate DSP. Sampling rate converters, Sub-band encoder.


Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:
M TECH: VLSI DESIGN

VD-721 (ELECTIVE-III) MIXED-SIGNAL IC DESIGN

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Data Converters: Introduction, Characteristic Parameters, Basic DAC and ADC Architectures.
Sampling and Aliasing, SPICE models for DACs and ADCs, Quantization Noise

Data Converter SNR: Clock Jitter, Improving SNR using Averaging, decimating filters for ADC’s, Interpolating filters for DAC’s, Band pass and high pass Sinc filters, using feedback to improve SNR.

Second order Noise Shaping, Noise shaping Topologies.

Implementing data converters: R-2R topologies for DAC’s – Current mode, voltage mode, wide swing current mode DAC, topologies without an op-amp, effects of op-amp parameters. Implementing ADC’s- Implementing S/H, Cyclic ADC, Pipeline ADC- using 1.5 bits per stage, capacitor error averaging, comparator placement, clock generation, offsets and alternative topologies, Layout of Pipelined ADC’s.

Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:


MACH/OS kernel architecture. OSF/1 architecture and applications.

**Note:** The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

**Recommended Books:**

M TECH: VLSI DESIGN

VD-725 (ELECTIVE-III) NEURAL NETWORKS

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours


Supervised Learning and Neurodynamics: Perceptron training rules, Delta, Back propagation training algorithm, Hopfield Networks, Associative Memories.

Unsupervised and Hybrid Learning: Principal Component Analysis, Self-organizing Feature Maps, ART networks, LVQ, Applications for VLSI Design

Applications of Artificial Neural Networks to Function Approximation, Regression, Classification, Blind Source Separation, Time Series and Forecasting.

Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:

M TECH: VLSI DESIGN

VD-722 (ELECTIVE-IV) MICRO ELECTRO MECHANICAL SYSTEMS

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Historical Background: Silicon Pressure sensors, Micromachining, MicroElectroMechanical Systems. Microfabrication and Micromachining: Integrated Circuit Processes, Bulk Micromachining: Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA) Physical Microsensors: Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples: Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors. Microactuators: Electromagnetic and Thermal microactuation, Mechanical design of microactuators, Microactuator examples, microvalves, micropumps, micromotors Microactuator systems: Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector. Surface Micromaching: One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon, Micromotors, Gear trains, Mechanisms. Application Areas: All- mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g DNA chip, micro-arrays. Lab/Design: (two groups will work on one of the following design project as a part of the course) RF/Electronics device/system, Optical/Photonic device/system, Medical device e.g. DNA-chip, micro-arrays.

Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:

M TECH: VLSI DESIGN

VD-724 (ELECTIVE-IV)  VLSI FOR WIRELESS COMMUNICATION

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours


Receiver Front End – Motivations - General Design Philosophy- Heterodyne and Other architectures – Filter Design - Band Selection Filter – Image Rejection Filter - Channel Filter - Non idealities and Design Parameters - Harmonic Distortion – Intermodulation -Cascaded Nonlinear Stages – Gain Compression – Blocking – Noise – Noise Sources -Noise Figure - Design of Front end parameter for DECT.


Note: The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

Recommended Books:

Beginning with a simple communication game – wrestling between safeguard and attack – Probability and Information Theory – Algebraic foundations – Number theory.


**Note:** The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.

**Recommended Books:**
LIST of Text Books for M TECH: VLSI DESIGN (Regular/ PartTime)

VD-611 SEMICONDUCTOR DEVICES MODELLING


VD-613 DIGITAL IC DESIGN


VD-615 EMBEDDED SYSTEM DESIGN


VD-612 HDLS AND FPGAS


VD-614 ANALOG IC DESIGN
VD-616  DIGITAL SIGNAL PROCESSING AND DSP ARCHITECTURES


VD-621  DIGITAL SYSTEM TESTING & TESTABLE DESIGN


VD-623 /624 Optimization Techniques


VD-711  ASYNCHRONOUS SYSTEM DESIGN

VD-713 Low-Power VLSI Design


VD-715 MEMORY DESIGN AND TESTING


VD-721 MIXED-SIGNAL IC DESIGN


VD-723 ADVANCED COMPUTER ARCHITECTURE


VD-725 NEURAL NETWORKS


**VD-712 RF INTEGRATED CIRCUITS**


**VD-714 ADVANCED COMPUTATIONAL METHODS**


**VD-716 FPGA - BASED SYSTEM DESIGN**


**VD-722 MICRO ELECTRO MECHANICAL SYSTEMS**


**VD-724 VLSI FOR WIRELESS COMMUNICATION**


**VD-726 /627 Research Methodology**

VD-726 CRYPTOGRAPHY & NETWORK SECURITY (PT)
