MEWAR UNIVERSITY CHITTORGARH (RAJASTHAN)

Faculty of Engineering and Technology

Scheme and Syllabus of

Master of Technology (Part-time)
VLSI Design

MEWAR UNIVERSITY CHITTORGARH (RAJASTHAN)
Faculty of Engineering and Technology

Three – Year (Part-time) M Tech: VLSI Design

Eligibility for Admission: A candidate for being eligible for admission to the Master of Technology in *VLSI Design* in the faculty of engineering and technology should have passed B.Sc. (Engg.)/ B.Tech/ B.E. or any other equivalent degree in the relevant discipline / branch from any recognized Indian or foreign University.

A candidate should have at least 55% marks or equivalent CGPA in the qualifying examination (50% marks or equivalent CGPA for Scheduled Caste/Scheduled Tribes Candidates) on the basis of which the admission is being sought.

Overview of the Programme: The normal duration of programme shall be Six Semesters for part-time students. A part time candidate shall mean a person employed in any government/ semi-government/ private organisation. The duration of the programme is extendable upto five years. However, in exceptional circumstances one-year extension may be granted with approval of the Vice-Chancellor of the University.

The complete programme comprises of 13 theory courses (09 Core and 04 elective) and 02 Lab courses followed by the dissertation in two phases. Student has to obtain at least 40 % marks to pass the examination (both internal and external examination separately) for all the courses specified in the scheme of the programme. The degree will be awarded on the basis of cumulative marks obtained in all the six semesters and the division obtained will be as under:

MEWAR UNIVERSITY CHITTORGARH (RAJASTHAN)
Scheme of Three – Year (Part-time) M Tech (VLSI Design)

First Semester

Course Code	Course Title	Contact Hours per week		Credit Hours	Internal Assessment/Examination		External Examination /Viva-voce	Total Marks
		L	P		Assignments /Lab Record	Teacher's Evaluation		
VD-611	Semiconductor Device Modelling	4	-	4	30	10	60	100
VD-613	Digital IC Design	4	-	4	30	10	60	100
VD-711/713/715	Elective-I	3	-	3	20	10	45	75
VD-617	Digital Design Lab	-	2	2	15	10	25	50
Total Semester Credits = 13					**Total Semester Marks = 325**			

Second Semester

Course Code	Course Title	Contact Hours per week		Credit Hours	Internal Assessment/Examination		External Examination /Viva-voce	Total Marks
		L	P		Assignments /Lab Record	Teacher's Evaluation		
VD-612	HDLs and FPGAs	4	-	4	30	10	60	100
VD-614	Analog IC Design	4	-	4	30	10	60	100
VD-712/714/716	Elective-II	3	-	3	20	10	45	75
VD-618	Analog Design Lab	-	2	2	15	10	25	50
Total Semester Credits = 13					**Total Semester Marks = 325**			

Third Semester

Course Code	Course Title	Contact Hours per week		Credit Hours	Internal Assessment/Examination		External Examination /Viva-voce	Total Marks
		L	P		Assignments /Lab Record	Teacher's Evaluation		
VD-615	Embedded Systems	4	-	4	30	10	60	100
VD-621	Digital system Testing & Testable Design	4	-	4	30	10	60	100
VD-721/723/725	Elective-III	3	-	3	20	10	45	75
Total Semester Credits = 11					**Total Semester Marks = 275**			

Fourth Semester

Course Code	Course Title	Contact Hours per week		Credit Hours	Internal Assessment/Examination		External Examination /Viva-voce	Total Marks
		L	P		Assignments	Teacher's Evaluation		
VD-616	Digital Signal Processing and DSP Architectures	4	-	4	30	10	60	100
VD-624	Optimization Techniques	4	-	4	30	10	60	100
VD-722/724/726	Elective-IV	3	-	3	20	10	45	75
Total Semester Credits = 11					**Total Semester Marks = 275**			

Fifth Semester

Course Code	Course Title	Contact Hours per week		Credit Hours	Internal Assessment/Examination		External Examination /Viva-voce	Total Marks
		L	P		Assignments / Report	Teacher/ Committee Evaluation		
VD – 627	Research Methodology	2	-	2	15	05	30	50
VD – 629	Dissertation (Phase-I)	-	6	6	75	75	-	150
Total Semester Credits = 08					**Total Semester Marks = 200**			

Sixth Semester

Course Code	Course Title	Contact Hours per week		Credit Hours	Internal Assessment/Examination		External Examination /Viva-voce	Total Marks
		L	P		Report	Teacher(s) Evaluation		
VD – 630	Dissertation (Phase-II)	-	10	10	50	-	200	250
Total Semester Credits = 10					**Total Semester Marks = 250**			

LIST OF ELECTIVES

ELECTIVE – I

1.	VD-711	Asynchronous System Design
2.	VD-713	Low-Power VLSI Design
3.	VD-715	Memory Design and Testing

ELECTIVE – II

1.	VD-712	RF Integrated Circuits
2.	VD-714	Advanced Computational Methods
3.	VD-716	FPGA Based System Design

ELECTIVE – III

1.	VD-721	Mixed Signal IC Design
2.	VD-723	Advanced Computer Architecture
3.	VD-725	Neural Networks

ELECTIVE – IV

1.	VD-722	Micro Electro Mechanical Systems
2.	VD-724	VLSI For Wireless Communication
3.	VD-726	Cryptography & Network Security

Internal Assessment/Examination: The internal evaluation for all theory courses (40% of the total marks) will be based on the evaluation of **three assignments** provided during the semester and assessment of the teacher concerned. Similarly, the internal evaluation for all Lab courses (50% of the total marks) will be based on the evaluation of lab record and assessment of the teacher concerned.

External Examination/Viva -voce: For all the theory courses, there will be **08 (Eight)** questions to be set by the external paper setter (nominated /approved by the competent authority) out of which the candidate will have to attempt **05 (Five)** questions all carrying equal marks. Duration of each external examination will be three hours. Similarly, the external evaluation for all Lab courses (50% of the total marks) will be based on the evaluation/viva-voce conducted by an external examiner (from the relevant field) nominated/approved by the competent authority.

Submission and Evaluation of Dissertation:

a) A dissertation supervisor (s) having at least post- graduate qualification, from industry/research organization shall be assigned to the student approved by the competent authority. *In no case, the candidate can have more than two dissertation supervisors.*
b) Dissertation work (Phase-I) in 5^{th} semester shall comprise of literature survey, problem formulation, finalization of goals to be achieved, outlines of the methodology to be used for achieving the targeted goals and final decision about S/W, H/W tools to be used for dissertation work in 6^{th} semester. The entire work will be documented in the form of report.
c) Internal assessment of dissertation (Phase-I) in 5^{th} semester will be made by the committee evaluating the report (50% weightage), oral presentation and response of the student in the discussion / presentation (50% weightage). The dissertation supervisor (s) shall be the member (s) of the committee.
d) The submission of dissertation (Phase-II) in 6^{th} semester shall be allowed only after ensuring that the research work carried out by the candidate has attained the level of satisfaction of the 'Dissertation Supervisor (s)' and proof of communication/acceptance of the research paper (if any, and certified in the report) in the relevant refereed journal/ conference.
e) The final dissertation external examination in 6^{th} semester shall be taken by a panel of examiners comprising of concerned Supervisor (s), one external examiner (from the relevant field) nominated/approved by the competent authority. Hard copies of dissertation, one for each supervisor (s), examiner and the university/ department, are required to be submitted by the student before the final dissertation external examination. The candidate shall appear before the examining committee for oral examination and presentation on the scheduled date.

M TECH: VLSI DESIGN

VD-611 SEMICONDUCTOR DEVICES MODELLING

Internal Assessment/Evaluation: 40 Marks
External Examination: 60 Marks
Duration of Examination: 03 Hours

Brief review of silicon devices & fabrication processes, Recent developments in microelectronic devices.

p-n junction- current flow mechanisms , DC , small signal, transient model under forward and reverse bias conditions, circuit models for different types of p-n junction diodes.

Bipolar junction transistor-current flow in BJT's, charge control models for BJT's, DC and small signal equivalent circuits, Gummel Poon mode, MEXTRAM model, HICUM model, second order effects- effects of non-uniform doping in the base, high injection, heavy doping effects in emitter, emitter crowding , non conventional BJT's- poly silicon emitter transistor, HBT.

MOSFETs: modeling of weak and strong inversion in three terminal and four terminal MOS transistors, effect of small dimensions- DIBL, charge sharing, channel length modulation, hot carrier effects. Small signal models of MOSFETs for low and medium frequencies, large signal modeling of MOS transistor in dynamic operation. Level 1, 2, 3, 4(BSIM) models, HSPICE Level 50 model.

Modeling for circuit simulation: types of models combining several effects into one physical model, parameter extraction, properties of good models

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- N. Dasgupta and A. Dasgupta, *Semiconductor Devices: Modeling and Technology*, PHI (2004).
- Y.Tsividis, *Operation and Modeling of The MOS Transistor*, OUP (2004).
- M. S. Tyagi, *Introduction to Semiconductor Materials and Devices*, Wiley, 1991.
- M. Shur, *Physics of Semiconductor Devices*, PH, 1990.
- D. Forty, *MOSFET Modeling with SPICE : Principles and Practices*, PH, 1997.
- B. G. Streetman, *Solid State Electronic Devices*, Fourth Edition, PH, 1995.
- R. Raghuram, *Computer Simulation for Electronic Circuits*, Wiley, 1989.
- W. Liu, *MOSFET Models for SPICE Including BSIM3v3 and BSIM4*, Wiley, 2001

M TECH: VLSI DESIGN

VD-613 DIGITAL IC DESIGN

Internal Assessment/Evaluation: 40 Marks
External Examination: 60 Marks
Duration of Examination: 03 Hours

Modeling of Interconnects: Interconnect parameters, wire models, SPICE models for wires. CMOS Inverter: Static and Dynamic Behavior, Power, Energy and Energy Delay, Technology scaling and its impact.

Design of CMOS Combinational Logic Gates: Static and dynamic CMOS Design, Speed and power dissipation in dynamic circuits, cascading of gates, designing logic for reduced supply voltages, simulation of logic circuits.

Design of CMOS Sequential Logic Circuits: Static and dynamic latches and registers, alternative register styles, pipelined sequential circuits, non-bistable sequential circuits.

Custom, Semi-custom, and Structured array design approaches: Cell Based Design – standard, compiled , macro cells, mega cells, ArrayBased Design – mask programmable and rewired arrays.

Coupling with Interconnects: Effects of Interconnect Parasitics, Advanced Interconnect techniques.

Timing issues in Digital Circuits: Timing classification, synchronous timing basics, sources of skew and jitter, clock distribution techniques, latch-based clocking, Self-timed circuit design, synchronizers and arbiters, clock synchronization using PLL.

Design of ALU- a case study: data paths, adder, multiplier, shifter, power and speed trade-off in data path structures, power management.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, *Digital Integrated Circuits : A Design Perspective*, Second Edition, PH/Pearson, 2003.
- S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits : Analysis and Design*, Third Edition, MH, 2002.
- N. Weste, K. Eshraghian and M. J. S. Smith, *Principles of CMOS VLSI Design : A Systems Perspective*, Second Edition (Expanded), AW/Pearson, 2001.
- J. P. Uyemura, *Introduction to VLSI Circuits and System*, Wiley, 2002.
- R. J. Baker, H. W. Li and D. E. Boyce, *CMOS Circuit Design, Layout and Simulation*, PH, 1997.

M TECH: VLSI DESIGN

VD-612 HDLS AND FPGAS

Internal Assessment/Evaluation: 40 Marks
External Examination: 60 Marks
Duration of Examination: 03 Hours

Verilog : basic concepts- Lexical conventions, data types, system tasks and compiler directives. Modules and ports. Gate level modeling- gate types, various types of gate delay specifications. Data flow modeling- assignments, delays, expressions, operators, . Behavioral modeling- structured procedures, procedural assignments, timing controls, conditional statements, loops, sequential and parallel blocks, generate blocks. Tasks and functions

FPGA Architectures and Technology. Historical background, channel type FPGA- Xilinx 3000 and Actel ACT2 family, structured programmable array logic, programming FPGAs, benchmarking of FPGAs. Recent developments- new architectures such as Altera FLEX, Pilkington (Motorola/ Toshiba), Xilinix XC4000, field programmable interconnect.

VHDL Synthesis for FPGA Implementation.: Mapping of statements to gate- assignment statements, logical, arithmetic and relational operators, vectors and slices, IF, Process, Case, Loop, Null, Wait statements. Modeling of flip-flops and latches. Modeling of FSM for synthesis. Some examples of synthesizable constructs.

Verilog Synthesis for FPGA Implementation: Verilog constructs and operators, interpretation of Verilog constructs, synthesis design flow- RTL to gates, translation, un-optimized intermediate representations, logic optimization, technology mapping and optimization, technology library, design constraints, optimized gate level description.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- S. Palnitkar, *Verilog HDL : A Guide to Digital Design and Synthesis*, PH/Pearson, 1996.
- K. Coffman, *Real World FPGA Design with Verilog*, PH, 2000
- P. J. Ashenden, *The Designer's Guide to VHDL*, Second Edition, Morgan Kaufmann, 2001.
- C. H. Roth, *Digital System Design with VHDL*, PWS/Brookscole, 1998.
- R. C. Seals and G. F. Whapshott, *Programmable Logic : PLDs and FPGAs*, MH, 1998.
- A,K. Sharma, *Programmable Logic Handbook : PLDs, CPLDs and FPGAs*, MH, 1998.

M TECH: VLSI DESIGN

VD-614 ANALOG IC DESIGN

Internal Assessment/Evaluation: 40 Marks
External Examination: 60 Marks
Duration of Examination: 03 Hours

Integrated CMOS Amplifiers: Why integrated CMOS, single stage amplifiers-common source amplifiers with different types of loads, source follower, common gate amplifiers, cascade stage, choice of device models, Differential amplifiers-analysis of single ended and differential output amplifiers, common mode response, differential pair with MOS load, gilbert cells.

Current Mirrors: Basic current mirriors, cascade current mirriors, analysis of current mirrors, Frequency response of amplifiers: general considerations, frequency response of different types of amplifiers, Sources of Noise in CMOS Amplifiers: types of noise, representation of noise, noise in amplifiers.

CMOS Band gap References: supply independent biasing, temperature independent references, PTAT current generation , constant G_m biasing , speed and noise issues, Comparators.

Feedback in Amplifiers: feedback topologies, effect of loading, effect of feedback on noise, CMOS Operational Amplifiers-performance parameters, one-stage and two-stage Op Amps, gain boosting, input range limitations, slew rate.

Switched Capacitor Circuits: sampling switches, speed and precision considerations, switched capacitor amplifier –unity gain buffer, switched capacitor common mode feedback, switched capacitor filters.

CMOS Phase Lacked Loops: simple PLLs, charge pump PLLs, non ideal effects in PLLs, applications in frequency multiplication, skew and jitter reduction.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- B. Razavi, *Design of Analog CMOS Integrated Circuits*, MH, 2001.
- P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Second Edition, OUP, 2002.
- R. Gregorian, *Introduction to CMOS Op-Amps and Comparators*, Wiley, 1999.
- K. R. Laker and W. M. C. Sansen, *Design of Analog ICs and Systems*, MH, 1994.

M TECH: VLSI DESIGN

VD-617 DIGITAL DESIGN LAB

Laboratory Experiments:

1. Design and simulation of 8-bit SISO and SIPO type registers modeled in VHDL and VERILOG, and synthesis on FPGA.
2. Circuit simulation of CMOS Inverter - study of static and dynamic behavior.
3. Design and simulation of 8-bit PISO and PIPO type registers modeled in VHDL and VERILOG, and synthesis on FPGA.
4. Study of the effect of variation in V_{DD} and Temperature on static and dynamic behavior of CMOS Inverter.
5. Design and simulation of 8:1 MUX modeled in VHDL and VERILOG, and synthesis on FPGA.
6. Comparison of transient response of dynamic NAND2 and dynamic NOR2 gates.
7. Design and simulation of 8-bit synchronous counter with LOAD, RESET, and up/down controls, modeled in VHDL and VERILOG, and synthesis on FPGA.
8. Layout design and characterization of master-slave DFF.
9. Design and simulation of 8-bit parity checker/generator modeled in VHDL and VERILOG, and synthesis on FPGA.
10. Layout design and characterization of NAND2 and NAND4 gates.
11. Design and simulation of 8:3 priority encoder, modeled in VHDL and VERILOG, and synthesis on FPGA.
12. Layout design and characterization of Transmission gate
13. Design and simulation of 4-digit decade counter, modeled in VHDL and VERILOG, and synthesis on FPGA.
14. Design and simulation of 4-bit combinational multiplier, modeled in VHDL and VERILOG, and synthesis on FPGA.
15. Design and simulation of 4-bit sequential multiplier, modeled in VHDL and VERILOG, and synthesis on FPGA.

M TECH: VLSI DESIGN

VD-618 ANALOG DESIGN LAB

Laboratory Experiments:

1. Design and simulation of CS, CG and CD amplifier.
2. Design of a p-n junction, BJT and MOSFET using different process parameters.
3. Design and simulation of MOSFET based basic and cascade current mirrors.
4. Study of dependence of SPICE parameters on process parameters for BJT.
5. Design and simulation of a differential MOSFET Amplifier.
6. Study of dependence of SPICE parameters on process parameters for a MOSFET.
7. Design and simulation of a single stage CMOS operational amplifier.
8. Layout design and simulation of a differential amplifier.
9. Design and simulation of positive TC and negative TC band gap reference.
10. Layout design and simulation of positive TC band gap reference.
11. Design and simulation of a second order switched capacitor filter.
12. Study of effect of short channel on SPICE parameters of a MOSFET.
13. Design and simulation of simple phase locked loop.
14. Design and simulation of charge pump phase locked loop.
15. Comparison of different device models using SPICE

M TECH: VLSI DESIGN

VD-615 EMBEDDED SYSTEM DESIGN

Internal Assessment/Evaluation: 40 Marks
External Examination: 60 Marks
Duration of Examination: 03 Hours

Introduction: Embedded Systems and Architectures. System integration, Hardware/Software Partitioning, Design Considerations and Trade-offs, Structural and behavioral descriptions.

Processors: ARM and SHARC processors- processor and memory organization, data operations, flow of control, input and output devices and primitives, busy-wait I/O, interrupts, supervisor mode, exceptions, traps. Memories: Caches, MMUs and address translation; CPU Performance: pipelining, super scaling execution, caching, CPU power consumption.

Interfaces and Communication Mediums: Bus protocols, DMA, system bus configurations, ARM Bus, SHARC Bus, Memory Devices- organization and types, I/O Devices-timers and counters, ADC and DACs, keyboards, LEDs, Displays and touch screens , Interfacings-memory and device interfacing. Designing with microprocessors.

Programming an Embedded System: Program design patterns for embedded systems, data flow and control/data flow graphs, analysis and optimization of execution time, energy, power, and program size. Processes: multiple tasks and processes, context switching, Operating Systems: Process state and Scheduling, O.S. structure, timing requirements on processes, interprocess communication and mechanisms.

Examples and Case Studies.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- W. Wolf, *Computers as Components : Principles of Embedded Computer Systems Design*, Morgan Kaufmann, 2000.
- F. Vahid and T. D. Givargis, *Embedded System Design: A Unified Hardware/Software Introduction*, Wiley, 2002.
- S. Heath, *Embedded Systems Design*, Second Edition, Butterworth-Heinemann, 2002.
- J. Catsoulis, *Designing Embedded Hardware*, ORA, 2002.
- J. J. Labrosse, *Embedded Systems Building Blocks*, CMP Books, 1999.
- G. De Micheli, R. Ernst and W. Wolf, *Readings in Hardware/Software Codesign*, Morgan Kaufmann, 2001.

VD-621 DIGITAL SYSTEM TESTING & TESTABLE DESIGN

Internal Assessment/Evaluation: 40 Marks
External Examination: 60 Marks
Duration of Examination: 03 Hours

Combinational ATPG. Current sensing based testing. Classification of sequential ATPG methods. Fault collapsing and simulation

Universal test sets. Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.

CMOS testing: Testing of static and dynamic circuits. Fault diagnosis: Fault models for diagnosis, Cause-effect diagnosis, Effect-cause diagnosis.

Design for testability: Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives.

Built-in self-test: Estimation of test length, Test points to improve testability, Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- *N. Jha & S.D. Gupta, Testing of Digital Systems, Cambridge, 2003.*
- *M. Abramovici etal, Digital System Testing and Testable Design, Computer Science Press, 1990*
- *P.K.LALA: Digital Circuit Testing and Testability, Academic Press, 1999.*
- *P.K.LALA: Self checking and Fault-tolerant Digital Design, Academic Press, 1999.*
- *M.L.BUSHNELL & V.D.AGARWAL: Essentials of Electronic Testing for Digital, Memory and Mixed signal VLSI circuits, Kluwer, 2000.*

M TECH: VLSI DESIGN

VD-616 DIGITAL SIGNAL PROCESSING AND DSP ARCHITECTURES

Internal Assessment/Evaluation: 40 Marks
External Examination: 60 Marks
Duration of Examination: 03 Hours

Implementations of Basic DSP Operations -Adders, Multipliers, Dividers; Discrete Fourier Transform Implementation-characteristics of DFT- direct implementation of DFT, fast fourier transforms; Fixed-Point versus Floating-Point Operations; Pipelining and Parallelism; Re-timing, Unfolding- algorithm, properties and applications of unfolding, Folding- folding transformation, register minimization in folded architectures, folding of multirate systems..

Systolic/Array Architectures-implementation of array processors, algorithmic representations, Mapping methods-mapping without changing the number of nodes and with reduced number of nodes, projection method, multiprojection, partitioning, projection of nodes with different operations; Programmable DSP Architectures-the architecture of standard computer, architectural approaches for DSP processors, characteristics of available DSPs, FIR filter program, DFT program, instruction pipelining, special arithmetic modules, on-chip memory; Memory Structures and Addressing.

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P-DSP's – Multiple access memory – Multi – port memory – VLIW architecture – pipelining – Special Addressing modes in P-DSP's – On Chip Peripherals.

TMS320C3X PROCESSOR :Architecture –Data formats – Addressing modes – Groups of addressing modes – Instruction sets – Operation – Block diagram of DSP starter kit – Application, Programs for processing real time systems – Generating and finding the sum of series, Convolution of two sequences , Filter design.

ADSP PROCESSORS :Architecture of ADSP-21XX and ADSP – 210XX series of DSP processors – Addressing modes and Assembly language instructions – Applications programs – Filter design, FFT calculation- Blackfin DSP Processor

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- P. Lapsley, J. Bier, A. Shoham and E. A. Lee, *DSP Processor Fundamentals : Architectures and Features*, Wiley/IEEE, 2001.
- P. Pirsch, *Architectures for Digital Signal Processing*, Wiley, 1998.
- T. Glokler and H. Meyr, *Design of Energy-Efficient Application Specific Instruction Set Processors*, Kluwer, 2004.
- B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture Programming and Application" -Tata McGraw – Hill Publishing Company Limited. New Delhi, 2008
- K. K. Parhi, *VLSI Digital Signal Processing Systems : Design and Implementation*, Wiley, 1999.
- V. K. Madisetti, *VLSI Digital Signal Processors*, Butterworth-Heinemann/IEEE Press, 1995.
- A. Bateman and I. Paterson-Stephens, *The DSP Handbook*, PH/Pearson, 2002.

- S. M. Kuo, *Digital Signal Processors : Architectures, Implementations and Applications*, PH/Pearson, 2004.
- L. Wanhammar, *DSP Integrated Circuits*, AP, 1999.
- B. Venkataramani and M. Bhaskar, *Digital Signal Processors : Architecture, Programming and Applications*, TMH, 2002.
- E. E. Swartzlander, *Application Specific Processors*, Kluwer, 1997.
- U. Meyer-Baese, *DSP with FPGAs*, Springer-Verlag, 2001.
- User guides Texas Instrumentation, Analog Devices, Motorola.

M TECH: VLSI DESIGN

VD-624 Optimization Techniques

Internal Assessment/Evaluation: 40 Marks
External Examination: 60 Marks
Duration of Examination: 03 Hours

Artificial Neural Networks (ANN): Objectives-History-Biological inspiration, Neuron model, Single input neuron, Multi-input neuron, Network architecture, Single layer of neurons, Multi-layers of Neurons.
Perceptron: Perceptron architecture, Stingle-neuron perceptron, Multi-neuron perceptron- Perceptron Learning Rule, Constructing learning rules, Training multiple neuron perceptrons

.**Associative Learning:** Simple associative network, Unsupervised Hebbrule- Hebb rule with decay, Instar rule, Kohonen rule.

Widro-Hoff Learning: Adaline Network, Single Adaline, Mean square Error, LMS algorithm, Analysis of Convergence.
Applications for VLSI Design
Applications of Artificial Neural Networks to Function Approximation, Regression, Time Series and Forecasting.
Genetic Algorithms (GA): Introduction, robustness of traditional optimization and search methods, goals of optimization, difference between genetic algorithms and traditional methods, a simple genetic algorithm, hand simulation, Grist for the search mill, similarity templates, learning the lingo.
GA Mathematical Foundations: Foundation theorem, schema processing, the two armed and k-armed bandit problem, schemata processing, building block hypothesis, minimal deceptive problem (MDP), extended schema analysis, MDP results, similarity templates as hyper planes.
GA Computer Implementation: Introduction, data structures, reproduction, crossover and mutation, a time to reproduce and a time to cross, main program and results, mapping objective functions to fitness form, fitness scaling, codings, a multiparameter mapped fixed point coding, discretization, constraints.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- Neural Network Design, PWS publishing company, 1995.
- Introduction to Artificial Neural Systems, Jaico Pub.House, Bombay, 1994.
- Neural Computing : Theory and practice, Van Nastrand Reinhold, 1989.
- Neural Networks – Algorithms, application and programming techniques, Addison Weley, 1991.
- D.E.Goldberg: Genetic Algorithms in search, optimization and machine teaching. Publisher: Addison Wesley.
- Anderson J.A., “An Introduction to Neural Networks”, PHI, 1999.
- Haykin S., “Neural Networks-A Comprehensive Foundations”, Prentice-Hall International, New Jersey, 1999.
- Freeman J.A., D.M. Skapura, “Neural Networks: Algorithms, Applications and Programming Techniques”, Addison-Wesley, Reading, Mass, (1992).

- Golden R.M., “Mathematical Methods for Neural Network Analysis and Design”, MIT Press, Cambridge, MA, 1996.
- Cherkassky V., F. Kulier, “Learning from Data-Concepts, Theory and Methods”, John Wiley, New York, 1998.
- Anderson J.A., E. Rosenfield, “Neurocomputing: Foundatiions of Research, MIT Press, Cambridge, MA, 1988.
- Kohonen T., “Self-Organizing Maps”, 2nd Ed., Springer Verlag, Berlin, 1997.
- Patterson D.W., “Artificial Neural Networks: Theory and Applications”, Prentice Hall, Singapore, 1995.
- Vapnik V.N., “Estimation of Dependencies Based on Empirical Data”, Springer Verlag, Berlin, 1982.

M TECH: VLSI DESIGN

VD-627 Research Methodology

Internal Assessment/Evaluation: 20 Marks
External Examination: 30 Marks
Duration of Examination: 03 Hours

Introduction to Educational Research :Concept, types – basic, applied and action, Need for educational research;
Reviewing Literature:Need, Sources – Primary and Secondary, Purposes of Review, Scope of Review, steps in conducting review.
Identifying and defining research problem: Locating, analysing stating and evaluating problem. Generating different types of hypotheses and evaluating them.
Methods of Research :Descriptive research design - survey, case study, content analysis, Ex-post Facto Research, Correlational and Experimental Research
Sampling Techniques:Concept of population and sample' sampling techniques - simple random sampling, stratified random sampling, systematic sampling and cluster sampling, snow ball sampling, purposive sampling, quota sampling techniques. determining size of sample.
Design and development of measuring instruments, Tests, questionnaires, checklists, observation schedules, evaluating research instruments, selecting a standardized test Procedure of data collection: Aspects of data collection, coding data for analysis.
Statistical Methods of Analysis :Descriptive statistics: Meaning, graphical representations, mean, range and standard deviation, characteristics and uses of normal curve. Inferential statistics: t-test, Chi-square tests, correlation (rank difference and product moment), ANOVA (one way), Selecting appropriate methods.
Procedure for writing a research proposal:Purpose, types and components of research proposal.
Procedure for writing a research report:Audiences and types of research reports, Format of research report and journal articles.
Strategies for evaluating, Research disseminating and utilising research – An Overview.
Practice Tasks

- Define a research problem in engineering education/industry after studying problem situation and literature
- Given the purpose, objectives of research, write hypotheses
- Select research designs for the given research objectives
- Identify the measuring instruments for the given research objectives/hypotheses
- Identify the appropriate statistical methods of analysis for the given research proposal.
- Critically analyse the given research reports on various aspects such as hypothesis, design, measuring tools, statistical analysis, interpretation etc. to identify the gaps or weaknesses in the study.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions*

Recommended Books:

- Borg, W and Gall, M. Educational Research: An Introduction, New York, Longman.2003
- Cohen, L. Educational Research in Classrooms and Schools ! A Manual of Materials and Methods NY: Harper and Row Publishers.2000
- CPSC: Developing Skills in Technician Education Research Modules 1 to 11 Singapore, Colombo Plan Staff College for Technician Education
- Garrett, HE and Woodworth, RS. Statistics in Psychology and Education, Educational Research, Bombay: Vakils Fetter and Simons Ltd. 2003
- Gay, LR, Educational Research, Ohio: Charles E. Merril Publishing Company2000
- Wiersma William Research Methods in Education – An Introduction London, Allyn and Bacon, Inc.2000

M TECH: VLSI DESIGN
VD – 629 DISSERTATION (PHASE-I)

Internal Assessment/Evaluation: 150 Marks

The primary objective of this course is to enhance the student ability to analyze and carry out independent investigations etc. Each student will carry out independent work which should involve creativity; innovation and ingenuity. A dissertation supervisor (s) having at least post- graduate qualification; from industry/research organization shall be assigned to the student approved by the competent authority. *In no case; the candidate can have more than two dissertation supervisors.* Industry oriented projects may be encouraged for the purpose.

The whole Dissertation work will be carried out and reported in two phases in 5^{th} semester and 6^{th} semester. Dissertation work (Phase-I) in 5^{th} semester shall comprise of literature survey; problem formulation; finalization of goals to be achieved; outlines of the methodology to be used for achieving the targeted goals and final decision about S/W; H/W tools to be used for dissertation work in 6^{th} semester. The entire work will be documented in the form of report.

Internal assessment of dissertation (Phase-I) in 5^{th} semester will be made by the committee evaluating the report (50% weightage); oral presentation and response of the student in the discussion / presentation (50% weightage). The dissertation supervisor (s) shall be the member (s) of the committee.

M TECH: VLSI DESIGN
VD– 630 DISSERTATION (PHASE-II)

Internal Assessment/Evaluation: 50 Marks
External Examination: 200 Marks

The complete dissertation work shall comprise of literature survey; problem formulation; methodology used; S/W; H/W tools used; Results and discussion followed by the conclusions & further scope of work in that area. The submission of dissertation in 6th semester shall be allowed only after ensuring that the research work carried out by the candidate has attained the level of satisfaction of the 'Dissertation Supervisor (s)' and proof of communication/acceptance of the research paper (if any; and certified in the report) in the relevant refereed journal/ conference.

The final dissertation external examination in 6th semester shall be taken by a panel of examiners comprising of concerned Supervisor (s); one external examiner (from the relevant field) nominated/approved by the competent authority. Hard copies of dissertation; one for each supervisor (s); examiner and the university/ department; are required to be submitted by the student before the final dissertation external examination. The candidate shall appear before the examining committee for oral examination and presentation on the scheduled date.

M TECH: VLSI DESIGN

VD-711 (ELECTIVE-I) ASYNCHRONOUS SYSTEM DESIGN

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Fundamentals: Handshake protocols, Muller C-element, Muller pipeline, Circuit implementation styles, theory. Static data-flow structures: Pipelines and rings, Building
blocks, examples

Performance: A quantitative view of performance, quantifying performance, Dependency graphic analysis. Handshake circuit implementation: Fork, join, and merge, Functional blocks, mutual exclusion, arbitration and metastability.

Speed-independent control circuits: Signal Transition graphs, Basic Synthesis Procedure, Implementation using state-holding gates, Summary of the synthesis Process, Design examples using Petrify. Advanced 4-phase bundled data protocols and circuits: Channels and protocols, Static type checking, More advanced latch control circuits.

High-level languages and tools: Concurrency and message passing in CSP, Tangram program examples, Tangram syntax-directed compilation, Martin's translation process, Using VHDL for Asynchronous Design. An Introduction to Balsa: Basic concepts, Tool set and design flow, Ancillary Balsa Tools

The Balsa language: Data types, Control flow and commands, Binary/Unary operators, Program structure. Building library Components: Parameterized descriptions, Recursive definitions. A simple DMA controller: Global Registers, Channel Registers, DMA control structure, The Balsa description.

Principles of Asynchronous Circuit Design - Jens Sparso, Steve Furber, Kluver Academic Publishers.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- Asynchronous Circuit Design- Chris. J. Myers, John Wiley & Sons,2001.
- Handshake Circuits An Asynchronous architecture for VLSI programming – Kees Van Berkel Cambridge University Press, 2004
- Principles of Asynchronous Circuit Design-Jens Sparso, Steve Furber, Kluver Academic Publishers, 2001.

M TECH: VLSI DESIGN

VD-713 (Elective-I) Low-Power VLSI Design

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Introduction: Sources of power dissipation, important parameters for low power design, Low power design approaches.

Transistor sizing vs. dissipation and speed, effect of scaling, Process Technology and Integration-Low power CMOS/BiCMOS Process, Low power SOI CMOS, Low Power Lateral BJT on SOI, LVLP CMOS Transistor structure via Poly profile Engineering.

Low power circuit techniques: Flip flops and Latches, Logic, High Capacitance Nodes. Energy Recovery CMOS: Retractile Logic, Reversible pipelines, High performance approaches.

Low power clock distribution: Power Distribution in Clock Distribution, Single driver vs. Distributed buffers, Buffer and device sizing, Zero skew vs. tolerant Skew, Chip and package Co-design of Clock Network.

Logic synthesis for low power: Power estimation Techniques, Power Minimization Techniques.

Design of low power arithmetic and memory elements: Circuit Design Style, Design of circuits for addition, Multiplication, Division.

Low power microprocessor Design – system power management, architectural trade-offs, choosing supply voltage, low power clocking, implementation options for low power.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- J. M. Rabaey, M.Pedram, *Low Power Design Methodologies,* Kluwer-Academic Publn.(2002).
- J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, *Digital Integrated Circuits : A Design Perspective*, Second Edition, PH/Pearson, 2003.
- K. Roy and S. C. Prasad, *Low-Power CMOS VLSI Circuit Design*, Wiley, 2000.
- A. P. Chandrakasan and R. W. Brodersen, *Low Power Digital CMOS Design*, Kluwer, 1995.
- A. P. Chandrakasan and R. W. Broderson, *Low-Power CMOS Design*, IEEE Press, 1998.
- E. Sanchez-Sinencio and A. G. Andreou, *Low-Voltage/Low-Power Integrated Circuits and Systems : Low-Voltage Mixed Signal Circuits*, IEEE Press, 1999.

M TECH: VLSI DESIGN

VD-715 (ELECTIVE-I) MEMORY DESIGN AND TESTING

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Introduction to Semiconductor Memories and Technologies: Internal organization of memory chips, basic memory elements, memory types, trends in SRAM and DRAM design, Non-volatile memory technologies.

SRAM and DRAM Cell Design; basic structures-NMOS static/dynamic circuits, CMOS circuits, cell design.

Sense Amplifiers: Voltage and Current Sense Amplifiers; Reference Voltage Generation; Voltage Converters.

Cache Memory Design.: concept of locality in space and time, interfacing cache memory with CPU, associated problems-parasitic capacitances, critical timing paths, bus turnaround.

Memory Testing: Reliability-failure mechanisms for memories, reliability modeling and fault detection, Yield, Radiation Effects-radiation types effecting the memory, radiation hardening techniques.

Memory chip design: a case study

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- K. Itoh, *VLSI Memory Chip Design*, Springer-Verlag, 2001.
- B. Keeth and R. J. Baker, *DRAM Circuit Design : A Tutorial*, Wiley/IEEE, 2000.
- B. Prince, *Semiconductor Memories : A Handbook of Design, Manufacture and Application*, Second Edition, Wiley, 1996.
- B. Prince, *High Performance Memories*, Wiley, 1999.
- B. Prince, *Emerging Memories : Technologies and Trends*, Kluwer, 2002.
- A. K. Sharma, *Advanced Semiconductor Memories : Architectures, Designs and Applications*, Wiley/IEEE, 2002.
- T. P. Haraszti, *CMOS Memory Circuits*, Kluwer, 2000.
- J. Handy, *The Cache Memory Book*, Second Edition, AP, 1998.
- M. I. Elmasry, *Digital MOS Circuits II : with Applications to Processors and Memory Design*, IEEE Press, 1992.

M TECH: VLSI DESIGN

VD-712 (ELECTIVE-II) RF INTEGRATED CIRCUITS

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Active RF Components and their characteristic parameters:RF diodes, BJT, FET, HEMT.

RF Filter Design: Filter configurations, resonators, filter realizations – Butterworth, Chebychev.

High-Frequency Amplifier Design: Zeros as bandwidth enhancer, shunt series amplifier, bandwidth enhancement with f_T doublers, voltage references and biasing, tuned and cascaded amplifiers, RF Power Amplifier Design.

Noise in RF Circuits: types of noise, two port noise theory, Low-Noise Amplifier (LNA) – intrinsic MOSFET two port noise parameters, LNA topologies, design example, LNA Design example.

Phase-Locked Loops: PLL models, noise properties, sequential phase detectors, loop filters and charge pumps. RF Oscillators: tuned and negative resistance oscillators. Mixers: non-linear systems as mixers, multiplier based mixers.

RF amplifier design – a case study

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, CUP, 1998.
- R. Ludwig and P. Bretchko, *RF Circuit Design*, Pearson, 2000.
- B. Razavi, *RF Microelectronics*, PH, 1998.
- B. Leung, *VLSI for Wireless Communication*, PH, 2002.
- B. Razavi, *Phase-Locking in High-Performance Systems*, Wiley/IEEE, 2003.
- B. Razavi, *Monolithic Phase-Locked Loops and Clock Recovery Circuits*, IEEE Press, 1996.
- R. E. Best, *Phase-Locked Loops : Design, Simulation and Applications*, Fifth Edition, MH, 2003.

M TECH: VLSI DESIGN

VD-714 (ELECTIVE-II) ADVANCED COMPUTATIONAL METHODS

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Solution of two or more nonlinear equations by iterative methods (Picard and Newton's methods) Spline interpolation, cubic splines, Chebyshev polynomials, Minimax approximation.

Eigenvalues and vectors of a real symmetric matrix – Jacobi method. Eigenvalue problem for ordinary differential equations.

Numerical solution of a parabolic equation. Explicit method, simple implicit method and Crank-Nicholson method. Stability.

Numerical Solution of elliptic problems. Dirichlet and Neumann problems (Cartesian and Polar coordinates)

Numerical solution of hyperbolic equations. Explicit method. Method of characteristics. Stability.

The finite element method – Ritz, collocation and Galerkin methods. Boundary value problems for ordinary differential equations. Shape functions. Assembly of element equations.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- Smith G. D. "Numerical Solution of Partial Differential Equation", Oxford, 1965.
- Chapra, S.C, Canale R P "Numerical Methods for Engineers" 3rd Ed., McGraw-Hill 1998.
- Kreyszig, E, "Advanced Engineering Mathematics", John Wiley, 8th ed., 2002.
- Gerald, C.F., "Applied Numerical Analysis", 6th Ed., Pearson, 1999.
- Niyogi, P. "Numerical Analysis and Algorithms", TMH, 2003.
- Conte, S.D. de Boor, C. "Elementary Numerical Analysis" McGraw-Hill.
- Strang, G., Fix, G.J. "An Analysis of Finite Element Method" Prentice Hall, 1973.
- Jain M. K. "Numerical Solution of Differential Equations" Wiley Eastern 1979.

M TECH: VLSI DESIGN

VD-716 (ELECTIVE-II) FPGA - BASED SYSTEM DESIGN

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Multirate signal processing- Decimation and Interpolation. Spectrum of decimated and interpolated signals, Polyphase decomposition of FIR filters and its applications to multirate DSP. Sampling rate converters, Sub-band encoder.

Filter banks-uniform filter bank. direct and DFT approaches. Introduction to ADSL Modem. Discrete multitone modulation and its realization using DFT. QMF. Short time Fourier Transform Computation of DWT using filter banks. Implementation and verification on FPGAs.

DDFS- ROM LUT approach. Spurious signals, jitter. Computation of special functions using CORDIC. Vector and rotation mode of CORDIC. CORDIC architectures. Implementation and verification on FPGAs.

Block diagram of a software radio. Digital downconverters and demodulators Universal modulator and demodulator using CORDIC. Incoherent demodulation - digital approach for I and Q generation, special sampling schemes. CIC filters. Residue number system and high speed filters using RNS. Down conversion using discrete Hilbert transform. Undersampling receivers, Coherent demodulation schemes.

Speech coding- speech apparatus. Models of vocal tract. Speech coding using linear prediction. CELP coder. An overview of waveform coding. Vocoders. Vocoder attributes. Block diagrams of encoders and decoders of G723.1, G726, G727, G728 and G729.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- J. H. Reed, Software Radio, Pearson, 2002.
- U. Meyer – Baese , Digital Signal Processing with FPGAs, Springer, 2004
- Tsui, Digital Techniques for Wideband receivers, Artech House,2001.
- S. K. Mitra, Digital Signal processing, McGrawHill, 1998

M TECH: VLSI DESIGN

VD-721 (ELECTIVE-III) MIXED-SIGNAL IC DESIGN

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Data Converters: Introduction, Characteristic Parameters, Basic DAC and ADC Architectures. Sampling and Aliasing, SPICE models for DACs and ADCs, Quantization Noise

Data Converter SNR: Clock Jitter, Improving SNR using Averaging, decimating filters for ADC's, Interpolating filters for DAC's, Band pass and high pass Sinc filters, using feedback to improve SNR.

Noise Shaping data converters: SPICE model, First order noise shaping, First order Noise Shaping, - Digital first order NS Modulators, Modulation Noise,Decimating and filtering the output of a NS Modulator,Analog Sync filter using SPICE,Analog Implementation of First order NS Modulator, Feedback DAC,Effect of parameters of Integrator, Forward modulator, op-amp. Second order Noise Shaping, Noise shaping Topologies.

Implementing data converters: R-2R topologies for DAC's – Current mode,voltage mode, wide swing current mode DAC, topologies without an op-amp,effects of op-amp parameters. Implementing ADC's- Implementing S/H,Cyclic ADC, Pipeline ADC-using 1.5 bits per stage, capacitor error averaging,comparator placement, clock generation, offsets and alternative topologies, Layout of Pipelined ADC's.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- R. J. Baker, *CMOS Mixed Signal Cicuit Design*, Wiley/IEEE, 2002.
- A. Handkiewicz, *Mixed-Signal Systems : A Guide to CMOS Circuit Design*, Wiley-IEEE, 2002.
- B. Razavi, *Principles of Data Conversion System Design*, IEEE Press, 1995.
- P. V. A. Mohan, V. Ramachandran and M. N. S. Swamy, *Switched Capacitor Filters : Theory, Analysis and Design*, PH, 1995.
- E. Sanchez-Sinencio and A. G. Andreou, *Low-Voltage/Low-Power Integrated Circuits and Systems : Low-Voltage Mixed-Signal Circuits*, IEEE, 1999.
- Y. Tsividis, *Mixed Analog-Digital VLSI Devices and Technology*, MH, 1996.
- S. Rabii and B. A. Wooley, *Design of Low-Voltage Low-Power Sigma-Delta Modulators*, Kluwer, 1998.
- P. G. A. Jespers, *Integrated Converters : D-A and A-D Architectures, Analysis and Simulation*, OUP, 2001.
- R. Van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters*, Kluwer, 1994.

M TECH: VLSI DESIGN

VD-723 (ELECTIVE-III) ADVANCED COMPUTER ARCHITECTURE

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Multiprocessors and multi-computers. Multi-vector and SIMD computers. PRAM and VLSI Models. Conditions of parallelism. Program partitioning and scheduling. Program flow mechanisms. Parallel processing applications. Speed up performance law.

Advanced processor technology. Superscalar and vector processors. Memory hierarchy technology. Virtual memory technology. Cache memory organization. Shared memory organization.

Linear pipeline processors. Non linear pipeline processors. Instruction pipeline design. Arithmetic design. Superscalar and super pipeline design. Multiprocessor system interconnects. Message passing mechanisms.

Vector Processing principle. Multivector multiprocessors. .Compound Vector processing. Principles of multithreading. Fine grain multicomputers. Scalable and multithread architectures. Dataflow and hybrid architectures.

Parallel programming models. Parallel languages and compilers. Parallel programming environments. Synchronization and multiprocessing modes. Message passing program development. Mapping programs onto multicomputers. Multiprocessor UNIX design goals.

MACH/OS kernel architecture. OSF/1 architecture and applications.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- K. Hwang, Advanced Computer Architecture , TMH, 2001.
- W. Stallings, Computer Organization and Architecture, McMillan, 1990 .
- M.J. Quinn, Designing Efficient Algorithms for Parallel Computer, McGraw Hill, 1994.

M TECH: VLSI DESIGN

VD-725 (ELECTIVE-III) NEURAL NETWORKS

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Introduction: History, overview of biological Neuro-System, Mathematical Models of Neurons, ANN architecture, Learning rules, Learning Paradigms-Supervised, Unsupervised and reinforcement Learning.

Supervised Learning and Neurodynamics: Perceptron training rules, Delta, Back propagation training algorithm, Hopfield Networks, Associative Memories.

Unsupervised and Hybrid Learning: Principal Component Analysis, Self-organizing Feature Maps, ART networks, LVQ, Applications for VLSI Design

Applications of Artificial Neural Networks to Function Approximation, Regression, Classification, Blind Source Separation, Time Series and Forecasting.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- Anderson J.A., "An Introduction to Neural Networks", PHI, 1999.
- Haykin S., "Neural Networks-A Comprehensive Foundations", Prentice-Hall International, New Jersey, 1999.
- Freeman J.A., D.M. Skapura, "Neural Networks: Algorithms, Applications and Programming Techniques", Addison-Wesley, Reading, Mass, (1992).
- Golden R.M., "Mathematical Methods for Neural Network Analysis and Design", MIT Press, Cambridge, MA, 1996.
- Cherkassky V., F. Kulier, "Learning from Data-Concepts, Theory and Methods", John Wiley, New York, 1998.
- Anderson J.A., E. Rosenfield, "Neurocomputing: Foundatiions of Research, MIT Press, Cambridge, MA, 1988.
- Kohonen T., "Self-Organizing Maps", 2nd Ed., Springer Verlag, Berlin, 1997.
- Patterson D.W., "Artificial Neural Networks: Theory and Applications", Prentice Hall, Singapore, 1995.
- Vapnik V.N., "Estimation of Dependencies Based on Empirical Data", Springer Verlag, Berlin, 1982.

M TECH: VLSI DESIGN

VD-722 (ELECTIVE-IV) MICRO ELECTRO MECHANICAL SYSTEMS

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Historical Background: Silicon Pressure sensors, Micromachining, MicroElectroMechanical Systems. Microfabrication and Micromachining : Integrated Circuit Processes, Bulk Micromachining : Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA) Physical Microsensors: Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples: Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors. Microactuators: Electromagnetic and Thermal microactuation, Mechanical design of microactuators, Microactuator examples, microvalves, micropumps, micromotors Microactuator systems : Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector. Surface Micromaching : One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon, Micromotors, Gear trains, Mechanisms. Application Areas: All- mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Mecical devices e.g DNA chip, micro-arrays. Lab/Design: (two groups will work on one of the following design project as a part of the course) RF/Electronics device/system, Optical/Photonic device/system, Medical device e.g. DNA-chip, micro-arrays.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- Stephen D. Senturia, Microsystem Design, Kluwer Academic Publishers, 2001.
- Marc Madou, Fundamentals of Microfabrication, CRC Press, 1997.
- Gregory Kovacs, Micromachined Transducers Sourcebook, WCB McGraw-Hill, Boston, 1998.
- M-H. Bao, Elsevier, Micromechanical Transducers: Pressure sensors, accelerometers, and gyroscopes, New York, 2000

M TECH: VLSI DESIGN

VD-724 (ELECTIVE-IV) VLSI FOR WIRELESS COMMUNICATION

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Review of Modulation Schemes – BFSK- BPSK –QPSK – OQPSK – Classical Channel - Additive White Gaussian Noise – Finite Channel Bandwidth - Wireless Channel- Path Environment - Path Loss – Friis Equation – Multipath Fading – Channel Model - Envelope Fading – Frequency Selective Fading – Fast Fading - Comparison of different types of Fading- Review of Spread Spectrum – DSSS – FHSS - Basic Principle of DSSS - Modulation –Demodulation - Performance in the presence of noise- narrowband and wideband interferences.

Receiver Front End – Motivations - General Design Philosophy- Heterodyne and Other architectures – Filter Design - Band Selection Filter – Image Rejection Filter - Channel Filter - Non idealities and Design Parameters - Harmonic Distortion – Intermodulation -Cascaded Nonlinear Stages – Gain Compression – Blocking – Noise – Noise Sources -Noise Figure - Design of Front end parameter for DECT.

Low Noise Amplifier – Introduction - Matching Networks – Matching for Noise and Stability – Matching for Power – Implementation - Comparison of Narrowband and Wideband LNA - Wideband LNA Design - Narrowband LNA –Impedance matching -Power matching- Salient features of LNA –Core Amplifier Design.

Demodulators - Delta Modulators - Low Pass Sigma Delta Modulators – High Order Modulators - One Bit DAC and ADC –Passive Low Pass Sigma Delta Modulator - Band pass Sigma Delta Modulators – Comparison – PLL based Frequency Synthesizer - Loop Filter Design and Implementation.

Implementations: VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System - Efficient VLSI Architecture for Base Band Signal processing.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- Bosco Leung " VLSI for wireless Communication", Prentice Hall, 2002.
- Andreas F.Molisch " Wideband wireless Digital Communication", Prentice Hall PTR, 2001.
- George.V.Tsoulous "Adaptive Antennas for wireless Communication", IEEE Press, 2001.

- Xiaodong Wang and H.Vincent “Wireless Communication System ,Advanced Techniques for Signal Reception”, Pearson Education. 2004

M TECH: VLSI DESIGN

VD-726 (ELECTIVE-IV) CRYPTOGRAPHY & NETWORK SECURITY

Internal Assessment/Evaluation: 30 Marks
External Examination: 45 Marks
Duration of Examination: 03 Hours

Beginning with a simple communication game – wresting between safeguard and attack – Probability and Information Theory - Algebraic foundations – Number theory.

Substitution Ciphers - Transposition Ciphers - Classical Ciphers – DES – AES – Confidentiality Modes of Operation – Key Channel Establishment for symmetric cryptosystems.

Diffie-Hellman Key Exchange protocol – Discrete logarithm problem – RSA cryptosystems & cryptanalysis – ElGamal cryptosystem – Need for stronger Security Notions for Public key Cryptosystems – Combination of Asymmetric and Symmetric Cryptography – Key Channel Establishment for Public key Cryptosystems - Data Integrity techniques – Symmetric techniques - Asymmetric techniques

Authentication Protocols Principles – Authentication protocols for Internet Security – SSH Remote logic protocol – Kerberos Protocol – SSL & TLS – Authentication frame for public key Cryptography – Directory Based Authentication framework – Non - Directory Based Public-Key Authentication framework .

Protecting Programs and Data – Information and the Law – Rights of Employees and Employers – Software Failures – Computer Crime – Privacy – Ethical Issues in Computer Security.

Note: *The examiner is required to set EIGHT questions in all carrying equal marks covering the entire syllabus. The candidate is required to attempt FIVE questions.*

Recommended Books:

- Wenbo Mao “Modern Cryptography – Theory and Practice”, Pearson Education, First Edition, 2006.
- Douglas R. Stinson “Cryptography Theory and Practice ”, Third Edition, Chapman & Hall/CRC,2006.
- Charles B. Pfleeger, Shari Lawrence Pfleeger “Security in Computing”, Fourth Edition, Pearson Education, 2007.
- Wade Trappe and Lawrence C. Washington “Intrduction to Cryptography with Coding Theory” Second Edition, Pearson Education, 2007.

LIST of Text Books for M TECH: VLSI DESIGN (Regular/ PartTime)

VD-611 SEMICONDUCTOR DEVICES MODELLING

1. N. Dasgupta and A. Dasgupta, *Semiconductor Devices: Modeling and Technology*, PHI (2004).
2. Y.Tsividis, *Operation and Modeling of The MOS Transistor*, OUP (2004).
3. M. S. Tyagi, *Introduction to Semiconductor Materials and Devices*, Wiley, 1991.
4. W. Liu, *MOSFET Models for SPICE Including BSIM3v3 and BSIM4*, Wiley, 2001

VD-613 DIGITAL IC DESIGN

1. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, *Digital Integrated Circuits : A Design Perspective*, Second Edition, PH/Pearson, 2003.
2. N. Weste, K. Eshraghian and M. J. S. Smith, *Principles of CMOS VLSI Design : A Systems Perspective*, Second Edition (Expanded), AW/Pearson, 2001.
3. J. P. Uyemura, *Introduction to VLSI Circuits and System*, Wiley, 2002.
4. R. J. Baker, H. W. Li and D. E. Boyce, *CMOS Circuit Design, Layout and Simulation*, PH, 1997.

VD-615 EMBEDDED SYSTEM DESIGN

1. W. Wolf, *Computers as Components : Principles of Embedded Computer Systems Design*, Morgan Kaufmann, 2000.
2. F. Vahid and T. D. Givargis, *Embedded System Design: A Unified Hardware/Software Introduction*, Wiley, 2002.
3. S. Heath, *Embedded Systems Design*, Second Edition, Butterworth-Heinemann, 2002.
4. J. Catsoulis, *Designing Embedded Hardware*, ORA, 2002.

VD-612 HDLS AND FPGAS

1. S. Palnitkar, *Verilog HDL : A Guide to Digital Design and Synthesis*, PH/Pearson, 1996.
2. P. J. Ashenden, *The Designer's Guide to VHDL*, Second Edition, Morgan Kaufmann, 2001.
3. C. H. Roth, *Digital System Design with VHDL*, PWS/Brookscole, 1998.

VD-614 ANALOG IC DESIGN

1. B. Razavi, *Design of Analog CMOS Integrated Circuits*, MH, 2001.
2. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Second Edition, OUP, 2002.

VD-616 DIGITAL SIGNAL PROCESSING AND DSP ARCHITECTURES

1. P. Lapsley, J. Bier, A. Shoham and E. A. Lee, *DSP Processor Fundamentals : Architectures and Features*, Wiley/IEEE, 2001.
2. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture Programming and Application" -Tata McGraw – Hill Publishing Company Limited. New Delhi, 2008
3. K. K. Parhi, *VLSI Digital Signal Processing Systems : Design and Implementation*, Wiley, 1999.
4. S. M. Kuo, *Digital Signal Processors : Architectures, Implementations and Applications*, PH/Pearson, 2004.

VD-621 DIGITAL SYSTEM TESTING & TESTABLE DESIGN

1. N. Jha & S.D. Gupta, Testing of Digital Systems, Cambridge, 2003.
2. M. Abramovici etal, Digital System Testing and Testable Design, Computer Science Press, 1990
3. P.K.LALA: Digital Circuit Testing and Testability, Academic Press, 1999.
4. M.L.BUSHNELL & V.D.AGARWAL: Essentials of Electronic Testing for Digital, Memory and Mixed signal VLSI circuits, Kluwer, 2000.

VD-623 / 624 Optimization Techniques

1. Neural Network Design, PWS publishing company, 1995.
2. D.E.Goldberg: Genetic Algorithms in search, optimization and machine teaching. Publisher: Addison Wesley.
3. Freeman J.A., D.M. Skapura, "Neural Networks: Algorithms, Applications and Programming Techniques", Addison-Wesley, Reading, Mass, (1992).
4. Golden R.M., "Mathematical Methods for Neural Network Analysis and Design", MIT Press, Cambridge, MA, 1996.

VD-711 ASYNCHRONOUS SYSTEM DESIGN

1. Asynchronous Circuit Design- Chris. J. Myers, John Wiley & Sons,2001.

2. Handshake Circuits An Asynchronous architecture for VLSI programming – Kees Van Berkel Cambridge University Press, 2004
3. Principles of Asynchronous Circuit Design-Jens Sparso, Steve Furber, Kluver Academic Publishers, 2001.

VD-713 Low-Power VLSI Design

1. J. M. Rabaey, M.Pedram, *Low Power Design Methodologies,* Kluwer-Academic Publn.(2002).
2. K. Roy and S. C. Prasad, *Low-Power CMOS VLSI Circuit Design*, Wiley, 2000.
3. A. P. Chandrakasan and R. W. Broderson, *Low-Power CMOS Design*, IEEE Press, 1998.
4. E. Sanchez-Sinencio and A. G. Andreou, *Low-Voltage/Low-Power Integrated Circuits and Systems : Low-Voltage Mixed Signal Circuits*, IEEE Press, 1999.

VD-715 MEMORY DESIGN AND TESTING

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